



SANYO Semiconductors

DATA SHEET

LV4149W — Bi-CMOS LSI For LCD Panel Drive Single Chip IC

Overview

The LV4149W is single chip IC for LCD panel drive.

Functions

- Analog block RGB Decoder/Driver
- Digital block Timing Generator

Specifications

Absolute Maximum Ratings at $T_a = 25^\circ\text{C}$

| Parameter | Symbol | Conditions | Ratings | Unit |
|-----------------------------|-----------------------|--|----------------------|------------------|
| Maximum supply voltage | $V_{CC1 \text{ max}}$ | Analog LOW type | 6 | V |
| | $V_{CC2 \text{ max}}$ | Analog HIGH type | 12 | V |
| | $V_{DD \text{ max}}$ | Digital type | 4.5 | V |
| Allowable power dissipation | $P_d \text{ max}$ | $T_a \leq 75^\circ\text{C}$ * Mounted on a board. | 350 | mW |
| Operating temperature | T_{opr} | | -15 to +75 | $^\circ\text{C}$ |
| Storage temperature | T_{stg} | | -40 to +125 | $^\circ\text{C}$ |
| Input pin voltage | $V_{IN A0}$ | Analog input pin (other than pin 33) | -0.3 to V_{CC1} | V |
| | $V_{IN A1}$ | Analog input pin (33PIN) | -0.3 to 10 | V |
| | $V_{IN D0}$ | Digital input pin (other than pins 10, 11, and 12) | -0.3 to $V_{DD}+0.3$ | V |
| | $V_{IN D1}$ | Digital input pin (10, 11, 12PIN) | -0.3 to +4.5 | V |

* : Mounted on a board : 30×30×1.6mm³, glass epoxy board

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SANYO Semiconductor Co., Ltd.

TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

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Operating Ratings at Ta = 25°C

| Parameter | Symbol | Conditions | Ratings | Unit |
|----------------------------------|--------------------|------------------|------------|------|
| Recommended supply voltage | V _{CC1} | Analog LOW type | 3.0 | V |
| | V _{CC2} | Analog HIGH type | 7.0 | V |
| | V _{DD} | Digital type | 3.0 | V |
| Operating voltage range | V _{CC1op} | Analog LOW type | 2.7 to 3.6 | V |
| | V _{CC2op} | Analog HIGH type | 6 to 9.5 | V |
| | V _{DDop} | Digital type | 2.7 to 3.6 | V |
| Recommended signal input voltage | RGBin | Pedestal - white | 0.35 | Vp-p |

Electrical DC Characteristics

Unless otherwise specified, the setting 1 and 2 must be made.

Unless otherwise specified, V_{CC1} = 3V, V_{CC2} = V_{CCCOM} = 7V, GND1 = GND2 = GNDCON = 0, V_{DD1} = V_{DD2} = V_{DD0} = 3V, V_{SS1} = V_{SS2} = V_{SS0} = 0, Ta = 25°C

[Current Characteristics]

| Parameter | Symbol | Conditions | Ratings | | | Unit | |
|---|-------------------|---|---------|-----|-----|------|----|
| | | | min | typ | max | | |
| Current dissipation V _{CC1} | I _{CC11} | Enter SIG4 (V _L = 0mV) to (A). Measure the current value of I _{CC1} . | Normal | 9.5 | 14 | 18.5 | mA |
| | | | Standby | 1 | 1.5 | 2 | mA |
| Current dissipation V _{CC2} | I _{CC2} | Enter SIG4 (V _L = 0mV) to (A). Measure the current value of I _{CC2} . | Normal | 1.5 | 2.8 | 3.5 | mA |
| | | | Standby | 0 | 0.1 | 0.2 | mA |
| Current dissipation V _{DD} , logic | I _{DD1} | Enter SIG4 (V _L = 0mV) to (A). Measure the current value of I _{DD11} and I _{DD22} . I _{DD1} , I _{DD2} , I _{DD3} = I _{DD11} +I _{DD22} | Normal | 3.5 | 6.5 | 8.5 | mA |
| | I _{DD2} | | Standby | 3 | 6 | 8 | mA |
| | I _{DD3} | | Sleep | 2 | 2.6 | 3.5 | mA |

[Digital block input/output characteristics]

| Parameter | Symbol | Conditions | Ratings | | | Unit |
|-----------------------------|------------------|--|--------------------|-----|--------------------|------|
| | | | min | typ | max | |
| L-level input voltage | V _{IL} | Digital block input pin (Note 1) | | | 0.3V _{DD} | V |
| H-level input voltage | V _{IH} | Digital block input pin (Note 1) | 0.7V _{DD} | | | V |
| H-level output voltage | VOHT | V _{DD} = 3.0V I _{OH} = -1.0mA (Note 2) | 2.8 | | | V |
| L-level output voltage | V _{OL} | I _{OL} = 1.0mA (Note 2) | | | 0.3 | V |
| Output transition time | t _{TLH} | Load 30pF (see Fig. 2) | | | 30 | ns |
| | t _{THL} | | | | 30 | ns |
| Cross point time difference | ΔT | Load 30pF Measure CKH1 and CKH2.(see Fig. 3) | | | 10 | ns |
| CHK duty | DTYHC | Load 30pF Measure the duty of CKH1 and CKH2. | 47 | 50 | 53 | % |

(Note 1) Digital block input pins : LOAD, DATA, SCLK, VDIN, HDIN, CLPIN

(Note 2) Digital block output pin (pins 13 to 15 and 17 to 30)

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Electrical AC Characteristics (1)

Unless otherwise specified, the setting 1 and 2 must be made.

Unless otherwise specified, $V_{CC1} = 3V$, $V_{CC2} = V_{CCCOM} = 7V$, $GND1 = GND2 = GNDCON = 0$,

$V_{DD1} = V_{DD2} = V_{DD0} = 3V$, $V_{SS1} = V_{SS2} = V_{SS0} = 0$, $T_a = 25^\circ C$

Unless otherwise specified, measure non-inverted output for P TP40, TP43, TP45 outputs.

[RGB signal system]

| Parameter | Symbol | Conditions | Ratings | | | Unit |
|--|------------------|--|---------|------|------|------|
| | | | min | typ | max | |
| Input-output gain TYP | GTP | Enter SIG3 to (A) and measure the ratio between the output amplitude (white to black) and input amplitude of TP43. | 14 | 16 | 18 | dB |
| Input-output gain MIN | GMN | Enter SIG3 to (A) and measure the ratio between the output amplitude (white to black) and input amplitude of TP43. | -2 | 1 | 4.5 | dB |
| Input-output maximum gain, MAX | GMX | Enter SIG3 to (A) and measure the ratio between the output amplitude (white to black) and input amplitude of TP43. | 19.5 | 21.5 | 23.5 | dB |
| Frequency characteristics | FCH | Assume that the output amplitude of TP43 when SIG1 (0dB, 100kHz) is entered to (A) is 0dB. Change the input signal frequency to change and determine the frequency at which the output amplitude becomes -3dB. FCH when the serial bus LPF = HIGH and FCL when LPF = LOW | 3.5 | | | MHz |
| | FCL | | 2.5 | | | MHz |
| Input/output delay rate | TD | Enter SIG8 to (A). Measure the delay time from the input signal 2T pulse peak to the peak of TP43 non-inverted output. | 0 | 100 | 200 | ns |
| Antipole output DC voltage change amount | COMBMX | Measure TP38 output. DC $I_O = \pm 1mA$ COMBMX when COMB = 63 and COMBMN when COMB = 0 | 3.55 | | | V |
| | COMBMN | | | | 2.6 | V |
| Output DC voltage $V_{CC2} = 8.5V$ | VSDH | Measure the TP50 voltage by setting $V_{CC2} = 8.5V$ and SIG center level changeover = low voltage mode. | 3.4 | 3.5 | 3.6 | V |
| Output DC voltage $V_{CC2} = 7V$ | VSD | Measure the TP50 voltage by setting $V_{CC2} = 7V$ and SIG center level changeover = high voltage mode. | 3.4 | 3.5 | 3.6 | V |
| RGB signal output DC voltage $V_{CC2} = 8.5V$ | V_{OUTH} | Set $V_{CC2} = 8.5V$ and SIG center level changeover = low voltage mode and enter SIG4 ($V_L = 0mV$) into (A). Adjust the serial bus BRIGHT to set TP43 output to 3Vp-p and measure the DC voltage of TP40, TP43, and TP45. | 3.3 | 3.5 | 3.7 | V |
| RGB signal output DC voltage $V_{CC2} = 7V$ | V_{OUT} | Set $V_{CC2} = 7V$ and SIG center level changeover = high voltage mode, and enter SIG4 ($V_L = 0mV$) to (A). Adjust the serial bus BRIGHT to set the TP43 output to 3Vp-p and measure the DC voltage of TP40, TP43, and TP45. | 3.3 | 3.5 | 3.7 | V |
| RGB signal output DC voltage difference | ΔV_{OUT} | Determine the maximum of differences among measurements of TP40, TP43, and TP45 of V_{OUT} of previous item. | | 0 | 120 | mV |
| Brightness change rate | BRTMX | Measure the change rate of the black level of TP40, TP43, and TP45 outputs when SIG2 is entered to (A) and BRT is changed from 128 to 255. | 2 | 2.5 | | V |
| | BRTMN | Measure the change rate of the white level of TP40, TP43, and TP45 outputs when SIG2 is entered to (A) and BRT is changed from 128 to 0. | | -2.5 | -2 | V |
| Antipole output change amount | COMWMX | Measure the difference between non-inverted and inverted levels of TP38 output when (A) = SIG2 is entered and COMW is set to 255. | 4.6 | | | V |
| | COMWMN | Measure the difference between non-inverted and inverted levels of TP38 output when (A) = SIG2 is entered and COMW is set to 0. | | | 0.1 | V |

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Continued from preceding page.

| Parameter | Symbol | Conditions | Ratings | | | Unit |
|---|--------|--|---------|------|-----|------|
| | | | min | typ | max | |
| Sub-brightness R change rates | SBBRTR | Measure the change amount of TP45 output black level when SIG2 is entered in (A) and COMW is changed from 128 to 255 and that of TP45 output white level change amount when COMW is changed from 128 to 0. | ±1.3 | ±1.7 | | V |
| Sub-brightness B change rates | SBBRTB | Measure the change amount of TP40 output black level when SIG2 is entered in (A) and COMW is changed from 128 to 255 and that of TP45 output white level when COMW is changed from 128 to 0. | ±1.3 | ±1.7 | | V |
| Gain difference between RGB signals | ΔGRGB | Determine the level difference of non-inverted output amplitude (white to black) of TP40, TP43, and TP45 when SIG3 is entered to (A). | -0.6 | 0 | 0.6 | dB |
| Sub-contrast R change rate | SBCNTR | Measure the non-inverted output (white to black) of TP45 for the non-inverted output (white to black) of TP43 when SIG3 is entered to (A) and when R-CNT = 0 and R-CNT = 255. | ±2.0 | | | dB |
| Sub-contrast B change rate | SBCNTB | Measure the non-inverted output (white to black) of TP40 for the non-inverted output (white to black) of TP43 when SIG3 is entered to (A) and when B-CNT = 0 and B-CNT = 255. | ±2.0 | | | dB |
| RGB inverted/non-inverted gain difference | ΔGINV | Determine the difference of inverted output amplitude for the non-inverted output amplitude (white to black) of TP40, TP43, and TP45 when SIG3 is entered to (A). | -0.5 | 0 | 0.5 | dB |

[RGB signal system]

| Parameter | Symbol | Conditions | Ratings | | | Unit |
|--|-------------------|--|---------|-----|-----|------|
| | | | min | typ | max | |
| Black level potential difference between RGB signals | ΔVBL | Determine the difference between highest and lowest black levels for inverted and non-inverted outputs of TP40, TP43, and TP45 when SIG3 is entered to (A). | | | 300 | mV |
| Gamma gain | G _{γL} | Enter SIG7 into (A) and set the non-inverted output amplitude (black and white) of TP43 at γ ₁ = 120, γ ₂ = 0 to 2.7Vp-p with CONT. Adjust the amplitude (black and white) to 3.5Vp-p with γ ₂ and the black level to 1.5V with BRT. Measure VG1, VG2 and VG3 and calculate as follows : G _{γL} = 20log (VG1/0.0357) G _{γM} = 20log (VG2/0.0357) G _{γH} = 20log (VG3/0.0357) (See Fig. 4.) | 23 | 26 | 29 | dB |
| | G _{γM} | | 12 | 15 | 18 | dB |
| | G _{γH} | | 23 | 26 | 29 | dB |
| γ ₁ adjustment variable range | V _{γ1MN} | Enter SIG7 to (A) and set the TP43 output (black to black) to 3Vp-p through BRIGHT adjustment. Read the γ gain change point at γ ₁ = 0, γ ₁ = 255 by referring to the IRE level of input signal : V _{γ1MN} for γ ₁ = 0 V _{γ1MX} for γ ₁ = 255 | | | 0 | IRE |
| | V _{γ1MX} | | 100 | | | IRE |
| γ ₂ adjustment variable range | V _{γ2MN} | Enter SIG7 to (A) and set the TP43 output (black to black) to 3Vp-p through BRIGHT adjustment. Read the γ gain change point at γ ₂ = 0, γ ₂ = 255 by referring to the IRE level of input signal : V _{γ2MN} for γ ₂ = 0 V _{γ2MX} for γ ₂ = 255 | 100 | | | IRE |
| | V _{γ2MX} | | | | 0 | IRE |
| Antipole transition time | tCOMH | Enter SIG3 to (A) and set the output amplitude of TP38 to 3Vp-p. Measure tCOMH for rise and tCOML for fall. Load : 1000pF | | 1 | 1.5 | μs |
| | tCOML | | | 1 | 1.5 | μs |
| RGB output black limiter variable range | VBLIMN | Enter SIG2 to (A) and measure the amplitude of the black side limiter of inverted/non-inverted TP38, 40, 43 and 45 output. | 4.5 | | | Vp-p |
| | VBLIMX | | | | 2 | Vp-p |
| RGB output white limiter variable range | VWLIMN | Enter SIG2 to (A) and measure the amplitude of the white side limiter of inverted/non-inverted TP38, 40, 43 and 45 output. | 4 | | | Vp-p |
| | VWLIMX | | | | 2.2 | Vp-p |

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| Parameter | Symbol | Conditions | Ratings | | | Unit |
|-------------------------|--------|--|---------|-----|-----|------|
| | | | min | typ | max | |
| Black limiter Dcvoltage | DVBLIM | Enter SIG4 ($V_L = 0mV$) to (A) and adjust BLIM to set the TP43 output to 3Vp-p. Measure the DC voltage of TP40, TP43, and TP45. | 3.3 | 3.5 | 3.7 | V |
| White limiter Dcvoltage | DVWLIM | Enter SIG4 ($V_L = 350mV$) into (A), measure the DC voltage of TP40, TP43, and TP45, and determine the difference from the above V_{OUT} . | 3.3 | 3.5 | 3.7 | V |

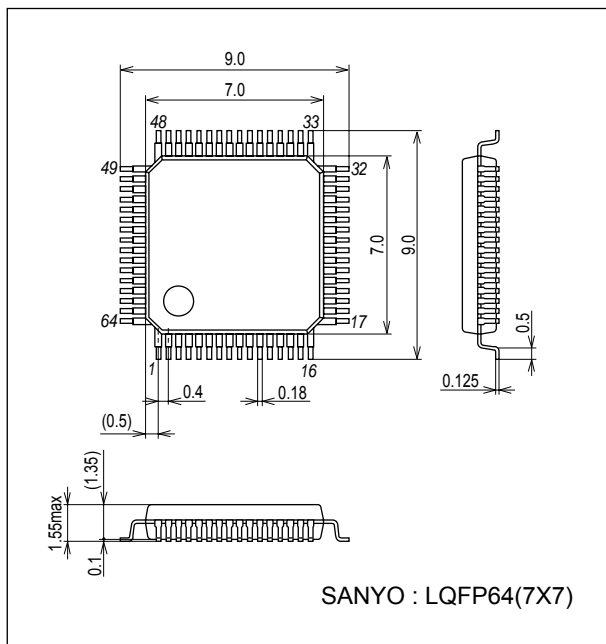
[Sync. separation, TG]

| Parameter | Symbol | Conditions | Ratings | | | Unit |
|-------------------------------------|--------|---|-----------|-----|-----|---------|
| | | | min | typ | max | |
| Input sync signal width sensitivity | WSSEP | Enter SIG4 ($V_L = 0mV$, $V_S = 143mV$, WS variable) to (A) and confirm synchronization with the TP15HD output. Narrow WS of SIG4 from 4.7 μs and determine WS at which synchronization between the input and TP15HD output is lost. | 2.0 | | | μs |
| Sync separation input sensitivity | VSSEP | Enter SIG4 ($V_L = 0mV$, $W_S = 4.7\mu s$, V_S variable) to (A) and confirm synchronization with the TP15HD output. Reduce V_S of SIG4 from 143mV and determine V_S at which synchronization between the input and TP15HD output is lost. | | 40 | 60 | mV |
| Sync separation output delay rate | TDSY1 | Enter SIG4 ($V_L = 0mV$, $W_S = 4.7\mu s$, $V_S = 143mV$) into (A) and measure the delay amount from the TP2RPD output. Assume that the period from fall of input HSYNC to a front edge of RPD output is TDSY1 and the period from rise of input HSYNC to the rear edge of RPD output is TDSY2. | 300 | 500 | 700 | ns |
| | TDSY2 | | 150 | 300 | 550 | ns |
| Horizontal pull-in range | HPLLN | Enter SIG4 ($V_L = 0mV$, $W_S = 4.7\mu s$, and $V_S = 143mV$, horizontal frequency variable) to (A) and confirm synchronization with TP15HD output. Determine the horizontal frequency f_H of SIG4 and calculate HPLLN = $f_H - 15734$ HPLLP = $f_H - 15625$. | ± 500 | | | Hz |
| | HPLLP | | ± 500 | | | Hz |

Package Dimensions

unit : mm (typ)

3281



Conditions of setting to measure the electric characteristic

Following settings must be made before measurement of electric characteristics.

Setting 1. System reset

Turn ON SW56 and start V56 from GND in order to perform system reset for MOS block.

(See fig. 1-1.)

The default value is set for the serial bus.

Setting 2. Horizontal AFC adjustment

Enter SIG4 ($V_L = 0mV$) to (A) and adjust VCOADJ so that the width of WL and WH becomes equal in the TP2 output waveform.(See fig 1-2.)

(Note) In order to measure the 2MHz or more band for measurement items, such as the RGB signal frequency characteristics, etc., it is necessary to pass through the sample hold circuit via serial bus.

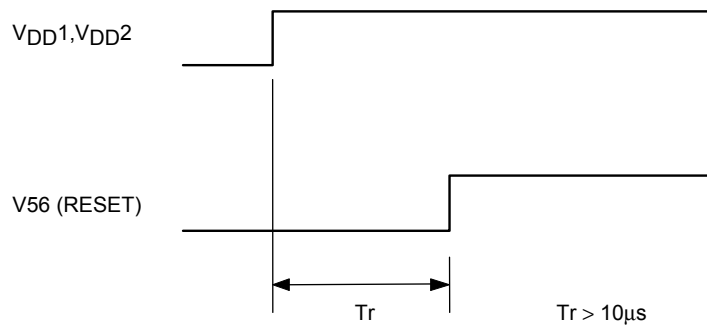


Fig.1-1 System reset

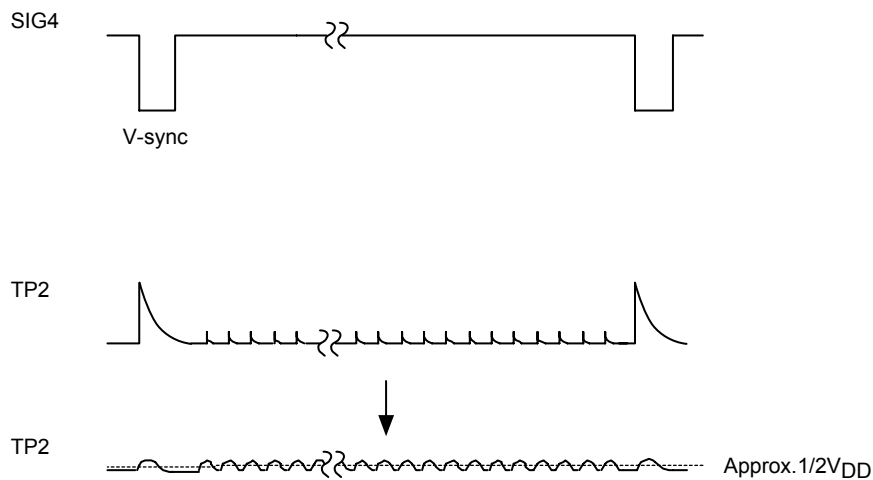


Fig.1-2 Horizontal AFC adjustment

Electric characteristics measurement method

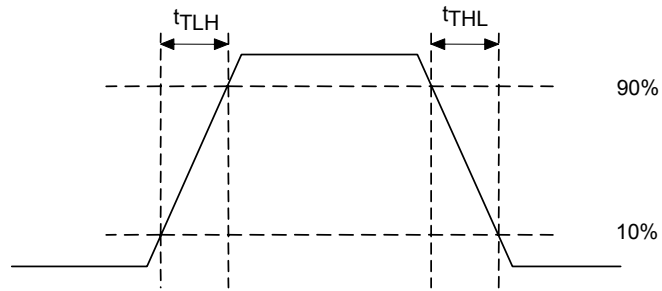


Fig.2 Output transition time measurement conditions

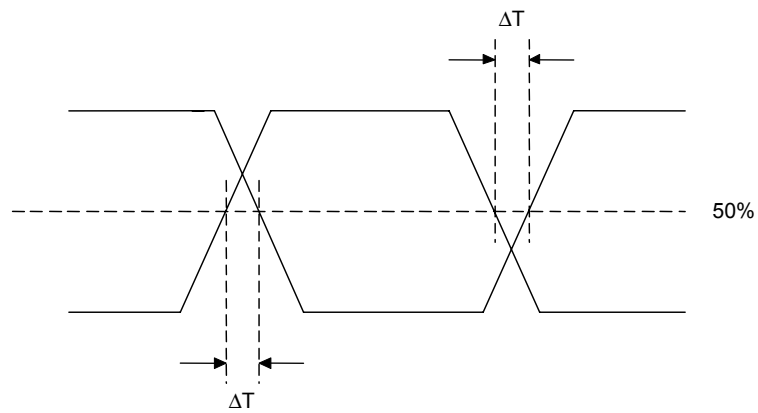


Fig.3 Cross point time difference measurement conditions

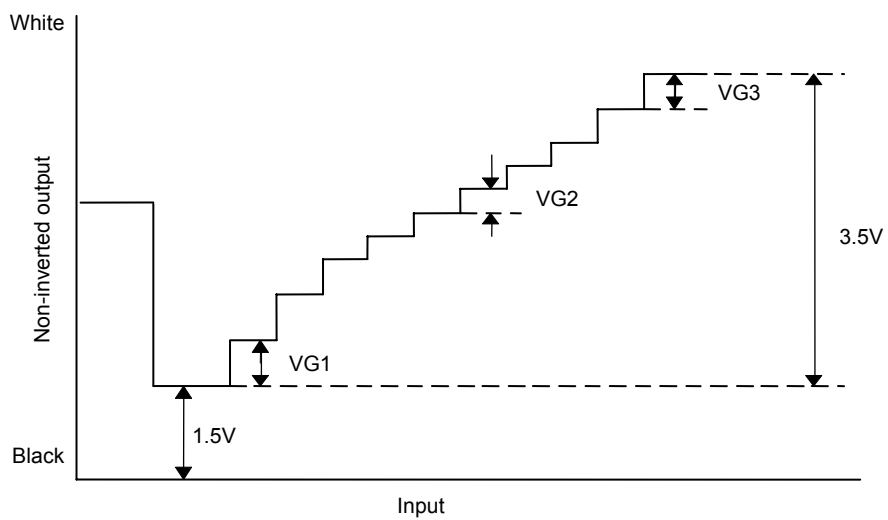
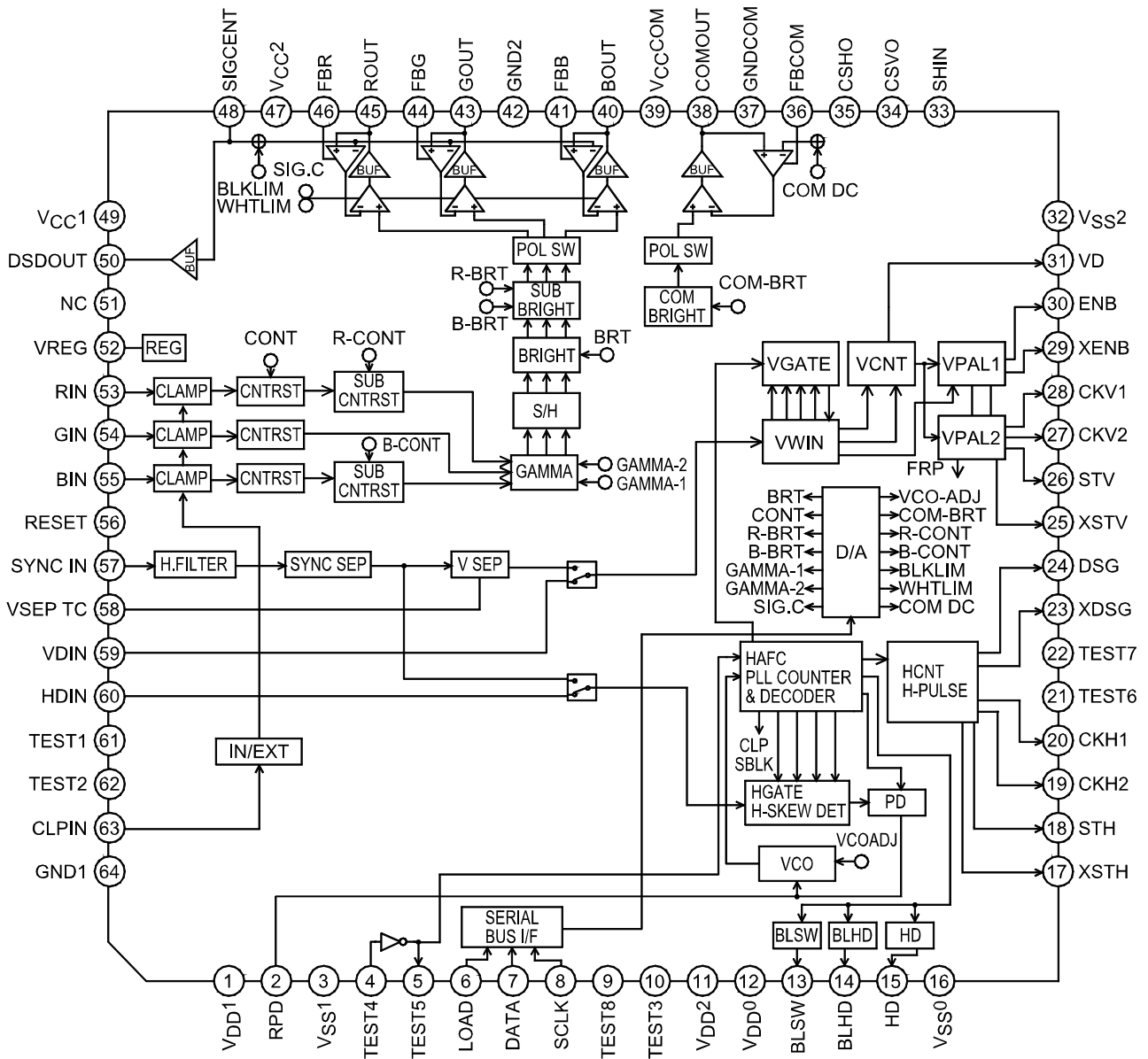


Fig.4 γ characteristics measurement conditions

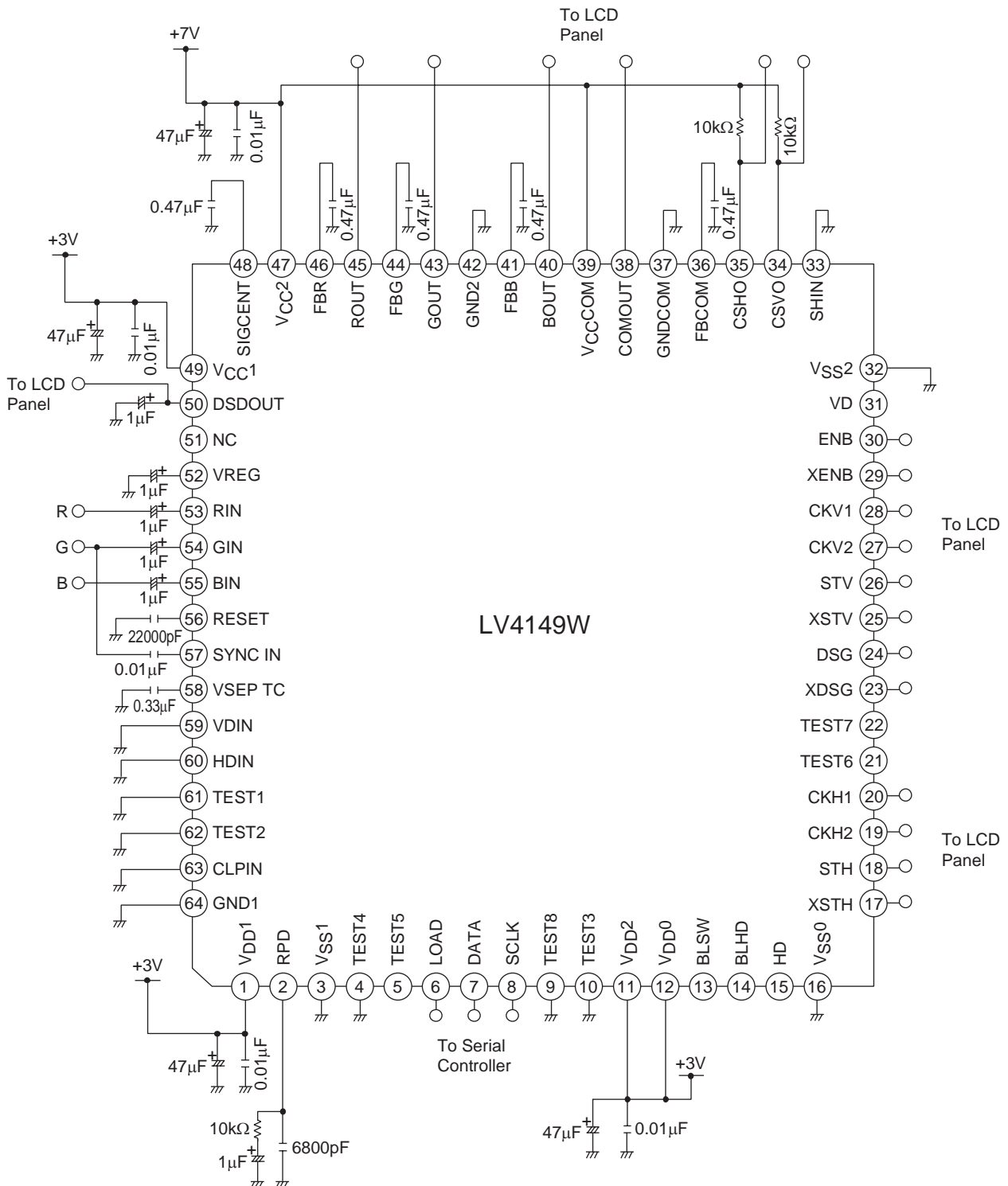
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Block Diagram



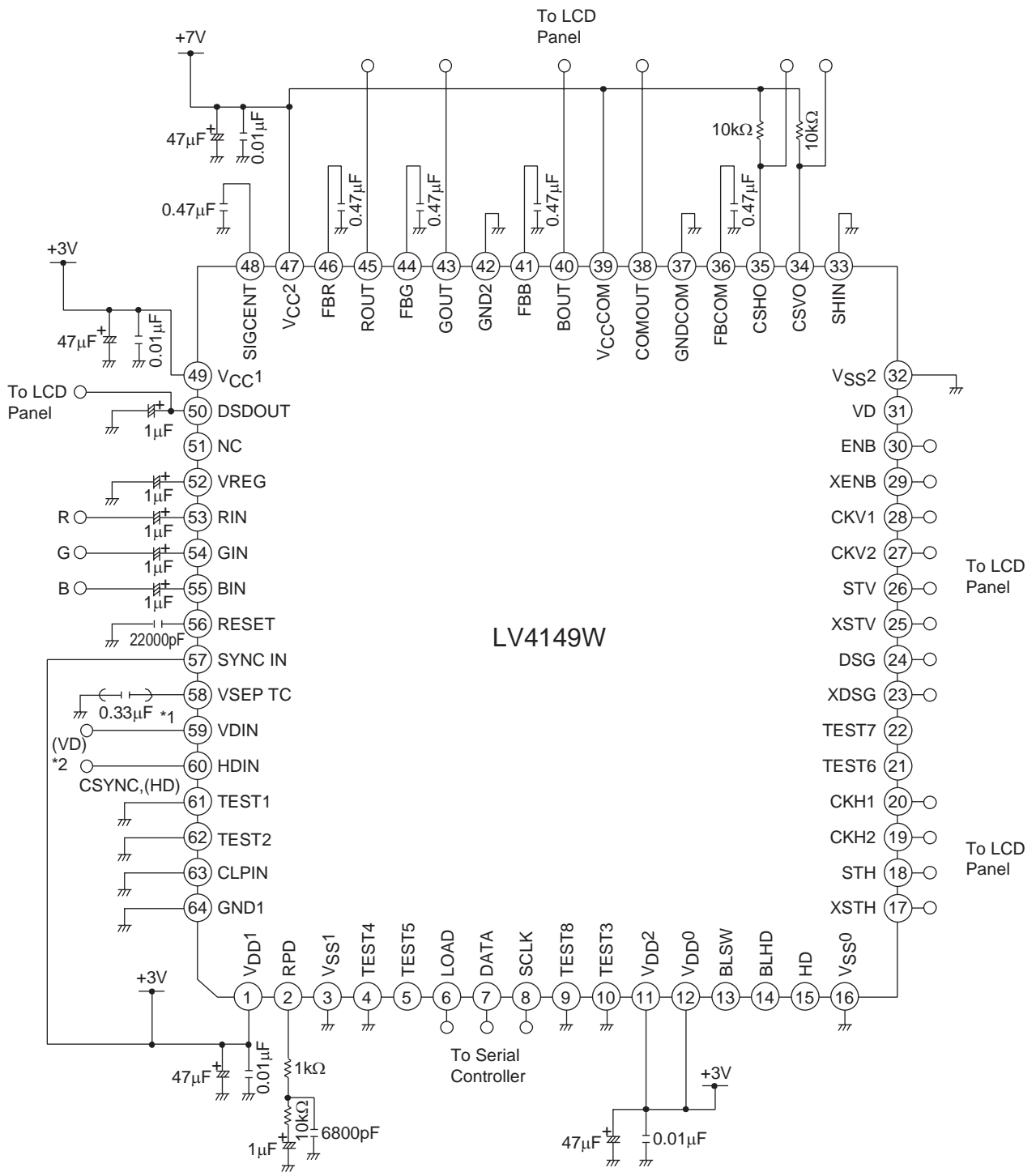
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Sampl Application Circuit (at input of internal synchronous separate signal)



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Sampl Application Circuit (at input of external synchronous separate signal)



*1 Delete (open) at input of external VD.

*2 Connect pin 59 to GND at input of composite sink

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Pin Description

| Pin No. | Pin Name | I/O | Pin Description |
|---------|--------------------|-----|---|
| 1 | V _{DD1} | - | Oscillation cell power supply (3V) |
| 2 | RPD | O | Phase comparison output |
| 3 | V _{SS1} | - | GND for oscillation cell |
| 4 | TEST4 | I | Oscillator cell input (also used for test) |
| 5 | TEST5 | O | Oscillator cell output |
| 6 | LOAD | I | Load input for serial bus |
| 7 | DATA | I | Data input for serial bus |
| 8 | SCLK | I | Clock input for serial bus |
| 9 | TEST8 | I | Test pin 8 |
| 10 | TEST3 | I | Test pin 3 |
| 11 | V _{DD2} | - | Digital system power supply (3V) |
| 12 | V _{DDO} | - | Digital output system power supply (3V) |
| 13 | BLSW | O | Backlight control pulse output |
| 14 | BLHD | O | Backlight drive pulse output |
| 15 | HD | O | H-drive output |
| 16 | V _{SSO} | - | Digital output system ground |
| 17 | XSTH | O | H-start pulse output (inverted) |
| 18 | STH | O | H-start pulse output |
| 19 | CKH2 | O | H-clock 2 pulse output |
| 20 | CKH1 | O | H-clock 1 pulse output |
| 21 | TEST6 | O | Test pin 6 |
| 22 | TEST7 | O | Test pin 7 |
| 23 | XDSG | O | Drain hold timing pulse output (inverted) |
| 24 | DSG | O | Drain hold timing pulse output |
| 25 | XSTV | O | V-start pulse output (inverted) |
| 26 | STV | O | V-start pulse output |
| 27 | CKV2 | O | V-clock 2 pulse output |
| 28 | CKV1 | O | V-clock 1 pulse output |
| 29 | XENB | O | Enable pulse output (inverted) |
| 30 | ENB | O | Enable pulse output |
| 31 | VD | O | V-drive pulse output(positive polarity) |
| 32 | V _{SS2} | - | Digital system ground |
| 33 | SHIN | I | Input pin for test |
| 34 | CSVO | O | Open collector output for vertical scan changeover |
| 35 | CSHO | O | Open collector output for lateral scan changeover |
| 36 | FBCOM | O | Time constant pin for antipole output DC return |
| 37 | GNDCOM | - | Antipole output ground |
| 38 | COMOUT | O | Antipole output |
| 39 | V _{CCCOM} | - | Power supply for antipole output (7V) |
| 40 | BOUT | O | B output |
| 41 | FBB | O | Time constant pin for B-output DC return |
| 42 | GND2 | - | 7V ground |
| 43 | GOUT | O | G output |
| 44 | FBG | O | Time constant pin for G-output DC return |
| 45 | ROUT | O | R output |
| 46 | FBR | O | Time constant pin for R-output DC return |
| 47 | V _{CC2} | - | 7V power supply |
| 48 | SIGCENT | I | Time constant pin for R, G, B, COM, and DSD output DC voltage |
| 49 | V _{CC1} | - | Analog 3V power supply |
| 50 | DSDOUT | O | Drain hold data output |
| 51 | NC | - | NC |
| 52 | VREG | - | Reference power supply |
| 53 | RIN | I | R signal input |
| 54 | GIN | I | G signal input |
| 55 | BIN | I | B signal input |

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| Pin No. | Pin Name | I/O | Pin Description |
|---------|----------|-----|---|
| 56 | RESET | I | System reset |
| 57 | SYNC IN | I | Sync signal input (composite) |
| 58 | VSEP TC | O | Time constant pin for separation of vertical sync |
| 59 | VDIN | I | VSYNC input |
| 60 | HDIN | I | CSYNC/HSYNC input |
| 61 | TEST1 | I | Test pin 1 |
| 62 | TEST2 | I | Test pin 2 |
| 63 | CLPIN | I | External clamp input |
| 64 | GND1 | - | Analog 3V power supply |

Analog pin function description

| Pin No. | Pin Name | Pin Voltage | Pin Description | Equivalent Circuit |
|----------------------|----------------------------|--------------|---|--------------------|
| 33 | SHIN | - | Input pin for test Normally, connect to the ground for use. | |
| 34 35 | CSVO CSHO | - | Vertical and horizontal inversion control output pin. Output is made from the open collector. Connect a resistor to CSVO and CSHO pins of the panel power supply. The resistance must comply with the panel specification. | |
| 36 41 44 46 | FBCOM FBR FBG FBB | 1.5V | Feedback circuit smoothing capacitor pin for control of antipole output DC level and RGB output DC level. Because of high impedance, a capacitor with small leakage is used. | |
| 37 | GNDCOM | 0V | Ground pin of antipole output | |
| 38 | COMOUT | 2.6 to 3.55V | Antipole AC output pin that can adjust the output DC voltage with variable resistor of serial bus. When the signal output DC voltage has been changed to $V_{CC2}/2$ and $V_{CC2} \cdot 21/51$ with the serial bus and the voltage has been applied to SIC.C from the outside, the DC voltage of antipole output follows. | |
| 39 | V _{CC} COM | 7V | Power pin of antipole output | |

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| Pin No. | Pin Name | Pin Voltage | Pin Description | Equivalent Circuit |
|----------------|----------------------|---------------------------------|---|--------------------|
| 40 43 45 | ROUT GOUT BOUT | $V_{CC2}/2$ $V_{CC2}^*21/51$ | RGB elementary color signal output pin. Can be changed to $V_{CC2}/2$ and $V_{CC2}^*21/51$ with the serial bus. | |
| 42 | GND2 | 0V | V_{CC2} ground. | |
| 47 | V_{CC2} | 7V | 7V power supply. | |
| 48 | SIGCENT | $V_{CC2}/2$ | Pin to set the DC voltage of R/G/B/COM/DSD output. Connect a capacitor of 0.01μF between this pin and GND2. When the signal output DC voltage is to be used with the setting other than $V_{CC2}/2$ and $V_{CC2}^*21/51$, set to the SIG center level changeover: high voltage mode with the serial bus and apply the voltage (3.3 - 3.7V) from the outside. | |
| 49 | V_{CC1} | 3.0V | Analog 3V power supply. | |
| 50 | DSDOUT | $V_{CC2}/2$ $V_{CC2}^*21/51$ | Drain hold data power output pin. The output DC voltage can be set to $V_{CC2}/2$ and $V_{CC2}^*21/51$ with the serial bus. Connect a capacitor of 1μF between this pin and GND2. | |
| 51 | NC | - | Pin not used | |
| 52 | VREG | 2.0V | Regulator output pin. Connect an external capacitor of 1μF or more. | |
| 53 54 55 | RIN GIN BIN | 1.45V | Analog RGB signal input pin. The standard input signal level is 0.5Vp-p (from sink chip to white 100%). Pedestal clamp is made with an external coupling capacitor. | |

Continued on next page.

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Continued from preceding page.

| Pin No. | Pin Name | Pin Voltage | Pin Description | Equivalent Circuit |
|---------|----------|-------------|---|--------------------|
| 56 | RESET | - | C-MOS circuit reset pin. Normally, this is used with the capacity connected to the ground. (Threshold value = 2.0V) | |
| 57 | SYNCIN | 1.6V | Input pin for sync separation. Input is made via the external capacitor. | |
| 58 | VSEPTC | 1.7V | Time constant connection pin for vertical sync separation. | |
| 64 | GND1 | - | Analog 3V power supply. | |

Digital pin function description

| Pin No. | Pin Name | Pin Voltage | Pin Description | Equivalent Circuit |
|---------|----------|-------------|---|--------------------|
| 1 | VDD1 | - | Power supply dedicated for VCO | |
| 2 | RPD | - | Phase comparator output pin | |
| 3 | VSS1 | 0 | Ground pin for VCO | |
| 4 | TEST4 | - | TEST4 is an input pin for test. | |
| 5 | TEST5 | - | TEST5 is an output pin for test. Use while fixing TEST4 to the ground potential and keeping TEST5 open. | |

Continued on next page.

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Continued from preceding page.

| Pin No. | Pin Name | Pin Voltage | Pin Description | Equivalent Circuit |
|--|--|-------------|---|--------------------|
| 6 7 8 | LOAD DATA SCLK | - | Serial bus input pin. Input possible up to 4.5V regardless of the V _{DD2} power voltage. | |
| 9 10 61 62 63 | TEST8 TEST3 TEST1 TEST2 CLPIN | - | TEST8, TEST3, TEST1, and TEST2 are input pins for test. Normally, this is used at the ground potential or in the open state. CLPIN is an input pin for external clamp. Use after setting to the external clamp input with the serial bus. Connect the CLPIN pin to the ground in cases other than external clamp input. | |
| 11 | V _{DD2} | - | Power pin for digital block | |
| 12 | V _{DD0} | - | Power pin for digital system output | |
| 13 14 15 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 | BLSW BLHD HD XSTH STH CKH2 CKH1 TEST6 TEST7 XDSG DSG XSTV STV CKV2 CKV1 XENB ENB VD | - | Digital output pin. | |
| 16 | V _{SS0} | - | Power pin for digital system output. Ground | |
| 32 | V _{SS2} | 0 | Digital ground pin. | |
| 59 60 | VDIN HDIN | - | External VD and HD input pins. When using, set them to the external synchronous signal input with the serial bus. Connect VDIN and HDIN pins to the ground in cases other than the external synchronous signal input. | |

| No. | Parameter | Symbol | Test Pin | Input signal, Conditions, etc. | SW set | | | | | | | | Mode set | | | DAC set | | | | | | | | | | | | |
|-----|--|------------------|----------|--------------------------------|--------|-----|-----|-----|----|----|----|----|----------|--------|-----|---------|-----|-----|-----|------------|------------|-----|------|------|-----|-----|-----|------|
| | | | | | 38 | 40 | 43 | 45 | 53 | 54 | 55 | 56 | Panel | System | SH | BRT | CNT | R-B | B-B | γ_1 | γ_2 | COM | RCNT | BCNT | BLM | WLM | VCO | COMB |
| | | | | | OFF | OFF | OFF | OFF | B | B | B | ON | - | - | ALL | 128 | 128 | 128 | 128 | 128 | 0 | 0 | 255 | 128 | 128 | 0 | 0 | ADJ |
| 23 | Antipole output change amount | COMMX | P38 | (A)=SIG2 | OFF | OFF | OFF | OFF | B | B | B | ON | - | - | ALL | 128 | 128 | 128 | 0 | 0 | 255 | 128 | 128 | 0 | 0 | ADJ | 51 | |
| 24 | Sub-brightness R change rate | COMWIN | P38 | (A)=SIG2 | OFF | OFF | OFF | OFF | B | B | B | ON | - | - | ALL | 128 | 128 | 128 | 0 | 0 | 128 | 128 | 128 | 0 | 0 | ADJ | 51 | |
| 25 | Sub-brightness B change rate | SBBRT | P41 | (A)=SIG4 | OFF | OFF | OFF | OFF | B | B | B | ON | - | - | ALL | 160 | 128 | 128 | 0 | 0 | 128 | 128 | 128 | 0 | 0 | ADJ | 51 | |
| 26 | Gain difference between RGB | SBBRTB | P45 | (A)=SIG4 | OFF | OFF | OFF | OFF | B | B | B | ON | - | - | ALL | 160 | 128 | 128 | 0 | 0 | 128 | 128 | 128 | 0 | 0 | ADJ | 51 | |
| 27 | Sub-contrast R change rate | Δ GRGB | | (A)=SIG3 | OFF | OFF | OFF | OFF | B | B | B | ON | - | - | ALL | 128 | 128 | 128 | 0 | 0 | 128 | 128 | 128 | 0 | 0 | ADJ | 51 | |
| 28 | Sub-contrast B change rate | SBCNTR | | (A)=SIG3 | OFF | OFF | OFF | OFF | B | B | B | ON | - | - | ALL | 128 | 70 | 128 | 128 | 0 | 0 | 128 | 128 | 128 | 0 | 0 | ADJ | 51 |
| 29 | RGB inverted/non-inverted gain | SBCNTB | | (A)=SIG3 | OFF | OFF | OFF | OFF | B | B | B | ON | - | - | ALL | 128 | 70 | 128 | 128 | 0 | 0 | 128 | 128 | 128 | 0 | 0 | ADJ | 51 |
| 30 | Black level potential difference between RGB signals | Δ GINV | | (A)=SIG3 | OFF | OFF | OFF | OFF | B | B | B | ON | - | - | ALL | 128 | 128 | 128 | 0 | 0 | 128 | 128 | 128 | 0 | 0 | ADJ | 51 | |
| 31 | Gamma gain | Δ VBL | | (A)=SIG3 | OFF | OFF | OFF | OFF | B | B | B | ON | - | - | ALL | 128 | 128 | 128 | 0 | 0 | 128 | 128 | 128 | 0 | 0 | ADJ | 51 | |
| 32 | γ_1 adjustment variable range | G γ L | P43 | (A)=SIG7 | OFF | OFF | OFF | OFF | B | B | B | ON | - | - | ALL | ADJ | ADJ | 128 | 128 | 120 | ADJ | 128 | 128 | 128 | 0 | 0 | ADJ | 51 |
| 33 | γ_2 adjustment variable range | G γ M | P43 | (A)=SIG7 | OFF | OFF | OFF | OFF | B | B | B | ON | - | - | ALL | ADJ | ADJ | 128 | 128 | 120 | ADJ | 128 | 128 | 128 | 0 | 0 | ADJ | 51 |
| 34 | Antipole transition time | G γ H | P43 | (A)=SIG7 | OFF | OFF | OFF | OFF | B | B | B | ON | - | - | ALL | ADJ | ADJ | 128 | 128 | 120 | ADJ | 128 | 128 | 128 | 0 | 0 | ADJ | 51 |
| 35 | RGB output black limiter operating voltage | V γ 1MN | P43 | (A)=SIG7 | OFF | OFF | OFF | OFF | B | B | B | ON | - | - | ALL | ADJ | 60 | 128 | 128 | 0 | 0 | 128 | 128 | 128 | 0 | 0 | ADJ | 51 |
| 36 | RGB output white limiter operating voltage | V γ 1MX | P43 | (A)=SIG7 | OFF | OFF | OFF | OFF | B | B | B | ON | - | - | ALL | ADJ | 60 | 128 | 128 | 255 | 0 | 128 | 128 | 128 | 0 | 0 | ADJ | 51 |
| 37 | Black limiter DC voltage difference | V γ 2MN | P43 | (A)=SIG7 | OFF | OFF | OFF | OFF | B | B | B | ON | - | - | ALL | ADJ | 60 | 128 | 128 | 0 | 0 | 128 | 128 | 128 | 0 | 0 | ADJ | 51 |
| 38 | White limiter DC voltage difference | V γ 2MX | P43 | (A)=SIG7 | OFF | OFF | OFF | OFF | B | B | B | ON | - | - | ALL | ADJ | 60 | 128 | 128 | 0 | 255 | 128 | 128 | 128 | 0 | 0 | ADJ | 51 |
| 39 | Input sync signal amplitude sensitivity | t _{COM} | P38 | (A)=SIG3 | ON | OFF | OFF | OFF | B | B | B | ON | - | - | ALL | 128 | 128 | 128 | 0 | 0 | ADJ | 128 | 128 | 128 | 0 | 0 | ADJ | 51 |
| 40 | Sync separation input sensitivity | t _{COM} | P38 | (A)=SIG3 | ON | OFF | OFF | OFF | B | B | B | ON | - | - | ALL | 128 | 128 | 128 | 0 | 0 | ADJ | 128 | 128 | 128 | 0 | 0 | ADJ | 51 |
| 41 | HD output delay rate | VBLIM | | (A)=SIG2 | OFF | OFF | OFF | OFF | B | B | B | ON | - | - | ALL | 0 | 128 | 128 | 0 | 0 | 128 | 128 | 128 | 0 | 0 | ADJ | 51 | |
| 42 | Horizontal pull-in range | VBLIMX | | (A)=SIG2 | OFF | OFF | OFF | OFF | B | B | B | ON | - | - | ALL | 0 | 128 | 128 | 0 | 0 | 128 | 128 | 128 | 255 | 0 | 0 | ADJ | 51 |
| | | VWLMN | | (A)=SIG2 | OFF | OFF | OFF | OFF | B | B | B | ON | - | - | ALL | 255 | 128 | 128 | 0 | 0 | 128 | 128 | 128 | 0 | 0 | ADJ | 51 | |
| | | VWLMX | | (A)=SIG2 | OFF | OFF | OFF | OFF | B | B | B | ON | - | - | ALL | 255 | 128 | 128 | 0 | 0 | 128 | 128 | 128 | 0 | 15 | ADJ | 51 | |
| | | Δ VBLIM | | (A)=SIG4 | OFF | OFF | OFF | OFF | B | B | B | ON | - | - | ALL | 0 | 128 | 128 | 0 | 0 | 128 | 128 | 128 | ADJ | 0 | ADJ | 51 | |
| | | Δ VWLM | | (A)=SIG4 | OFF | OFF | OFF | OFF | B | B | B | ON | - | - | ALL | 255 | 128 | 128 | 0 | 0 | 128 | 128 | 128 | 0 | 8 | ADJ | 51 | |
| | | VSSEP | | (A)=SIG4 | OFF | OFF | OFF | OFF | B | B | B | ON | - | - | ALL | 128 | 128 | 128 | 0 | 0 | 128 | 128 | 128 | 0 | 0 | ADJ | 51 | |
| | | VSSEP | | (A)=SIG4 | OFF | OFF | OFF | OFF | B | B | B | ON | - | - | ALL | 128 | 128 | 128 | 0 | 0 | 128 | 128 | 128 | 0 | 0 | ADJ | 51 | |
| | | TDSY1 | P15 | (A)=SIG4 | OFF | OFF | OFF | OFF | B | B | B | ON | - | - | ALL | 128 | 128 | 128 | 0 | 0 | 128 | 128 | 128 | 0 | 0 | ADJ | 51 | |
| | | TDSY2 | P15 | (A)=SIG4 | OFF | OFF | OFF | OFF | B | B | B | ON | - | - | ALL | 128 | 128 | 128 | 0 | 0 | 128 | 128 | 128 | 0 | 0 | ADJ | 51 | |
| | | HPLL | P15 | (A)=SIG4 | OFF | OFF | OFF | OFF | B | B | B | ON | - | - | ALL | 128 | 128 | 128 | 0 | 0 | 128 | 128 | 128 | 0 | 0 | ADJ | 51 | |
| | | HPLLP | P15 | (A)=SIG4 | OFF | OFF | OFF | OFF | B | B | B | ON | - | - | ALL | 128 | 128 | 128 | 0 | 0 | 128 | 128 | 128 | 0 | 0 | ADJ | 51 | |

(Note) PLL resetting necessary after change of the panel mode (- : arbitrary, ADJ : adjustment, SET : setting)

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Input sine wave (1)

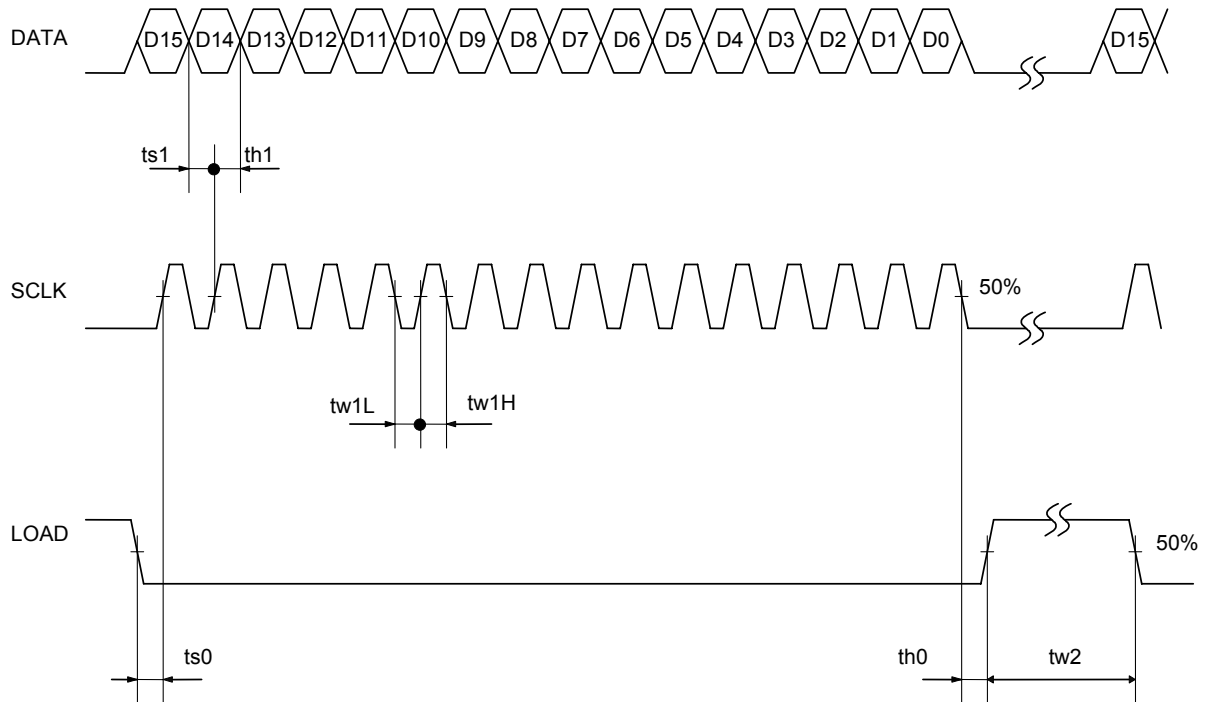
| SG No. | Sine wave | |
|--------|-----------|--|
| SIG1 | | With/without sine wave video signal (Amplitude and frequency variable) ← Value shown in the left 0dB |
| SIG2 | | |
| SIG3 | | 5-step staircase wave |
| SIG4 | | V_L amplitude variable V_S variable: 143mV, unless otherwise specified. W_S variable: 4.7 μ s, unless otherwise specified. f_H variable : NTSC 15.734kHz PAL 15.625kHz unless otherwise specified. |

Input sine wave (2)

| SG No. | Sine wave | |
|--------|-----------|--------------------------|
| SIG5 | | V_L amplitude variable |
| SIG6 | | Frequency variable |
| SIG7 | | 10-step staircase wave |
| SIG8 | | 2T pulse |

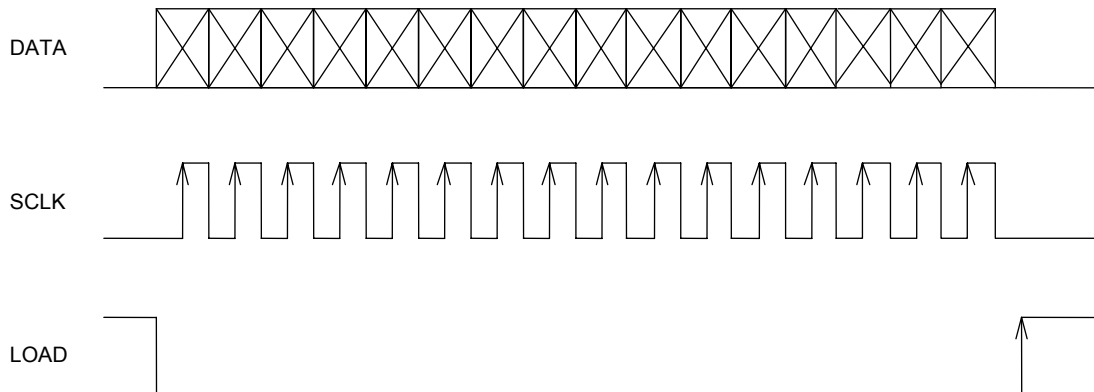
Serial bus communication specifications

(1) Conditions for serial transfer



| Parameter | Symbol | Conditions | min | typ | max | unit |
|------------------------|-----------|-------------------------------------|-----|-----|-----|---------|
| Serial transfer | | | | | | |
| Data setup time | ts_0 | LOAD setup time to start SCLK. | 150 | | | ns |
| | ts_1 | DATA setup time to start SCLK. | 150 | | | ns |
| Data hold time | th_0 | Hold time of LOAD for fall of SCLK. | 150 | | | ns |
| | th_1 | Data hold time to start SCLK. | 150 | | | ns |
| Pulse width | tw_{1L} | SCLK pulse width. | 160 | | | ns |
| | tw_{1H} | SCLK pulse width. | 160 | | | ns |
| | tw_2 | LOAD pulse width. | 1.0 | | | μ s |

(2) 3-wave serial format



Data length : 16bit

Clock frequency : 3MHz or less

When 16 clocks of "SCLK" are entered while "LOAD" is "L", "DATA" is taken at fall of "SCLK" and the operation is completed at rise of "LOAD."

(Note) If "SCLK" is 15 clocks or less while "LOAD" is "L", "DATA" is not taken. If "SCLK" is 17 clocks or more, "DATA" up to 16 clocks is taken and "DATA" beyond 16 clocks is not taken.

(3) Data output timing

1. Various mode settings

Some items (with a circle in the V latch column of data specification) have data set at fall of the vertical synchronous signal and some (without a mark in the V latch column) do not.

When data immediately before the vertical synchronous signal is transferred for multiple times, data immediately before vertical synchronous signal becomes effective for items to be set with the vertical synchronous signal. For items for which no setting is made, data becomes effective each time "DATA" is loaded.

2. Setting of the electric volume

D/A output data is changed at the same time with loading of "DATA."

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(4) Data specifications

(4-1) Various mode settings 1

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Description | V latch | Default |
|-----|-----|-----|-----|-----|-----|----|----|----|----|----|----|----|----|----|----|--|---------|---------|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | X | Not used | | (0) |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | LPF characteristic changeover : High | | ○ |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | LPF characteristic changeover : Low | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | X | 0 | 0 | Not used | | ○ |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | System changeover NTSC | | ○ |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | System changeover PAL | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | External VD input changeover OFF (used to separate IC sync) | | ○ |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | External VD input changeover ON (with external VD input) | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | X | X | X | 0 | 0 | 0 | 0 | 0 | Not used | | (000) |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | HD output polarity, positive | ○ | ○ |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | HD output polarity, negative | ○ | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | VD output polarity, positive | ○ | ○ |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | VD output polarity, negative | ○ | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Panel selection, 521×218 : (110,000 mode) | | ○ |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | Panel selection, 557×234 : (130,000 mode) | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | Not used | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | Panel selection, 320×240 : (70,000 mode) | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Field overlap method, odd number on even number | ○ | ○ |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | Field overlap method, even number on odd number | ○ | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Horizontal inversion, normal scan | ○ | ○ |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | Horizontal inversion, reverse scan | ○ | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Vertical inversion, from top to bottom | ○ | ○ |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | Vertical inversion, from bottom to top | ○ | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | X | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Not used | | (0) |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Normal mode | | ○ |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | For test. Do not set. | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | For test. Do not set. | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | For test. Do not set. | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | For test. Do not set. | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | X | 0 | 0 | 0 | Normal mode | | (0) |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | External SYNC input polarity change, negative polarity | | ○ |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | External SYNC input polarity, positive polarity | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | External clamp input changeover OFF (IC internal pulse used) | | ○ |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | External clamp input changeover ON (external pulse input) | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | HSYNC/CSYNC input changeover. SYNC IN valid | | ○ |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | HSYNC input changeover. HD IN valid | | |

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(4-1) Various mode settings 2

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Description | V latch | Default |
|-----|-----|-----|-----|-----|-----|----|----|----|----|----|-----|-----|-----|-----|-----|--|---------|------------|
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | X | Not used | | (0) |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | V gate ON | | ○ |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | V gate OFF | | ○ |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Normal mode | | ○ |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | For test. Do not set. | | ○ |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | X | 0 | 0 | 0 | Not used | | (0) |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | SIG center level changeover Low voltage | | ○ |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | SIG center level changeover High voltage | | ○ |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | X | X | X | 0 | 0 | 0 | 0 | 0 | Not use | | (000) |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | x | x | x | HC5 | HC4 | HC3 | HC2 | HC1 | H-position setting, 2fh×31Step (Note 1) | ○ | 10000 |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | x | x | x | x | 0 | VP2 | VP1 | VP0 | V-Position setting, 1H×6Step (Note 2) | ○ | 011 |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | x | x | x | x | X | 0 | 0 | 0 | Not used | | (0) |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | x | x | x | 0 | 0 | 0 | 0 | 0 | Monochrome EVF mode (at 70,000 mode) OFF | ○ | ○ |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | x | x | x | 1 | 0 | 0 | 0 | 0 | Monochrome ECF mode (at 70,000 mode) ON | ○ | |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | x | x | x | HD6 | HD5 | HD4 | HD3 | HD2 | HD phase setting, 4fh×31Step (Note 3) | ○ | 00000 |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | x | x | x | HW5 | HW4 | HW3 | HW2 | HW1 | BLHD pulse setting, 2fh×31Step (Note 4) | ○ | 10000 |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | X | X | X | X | X | X | X | X | Not used | | (00000000) |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | X | X | X | X | Not used | | (0000) |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | V blanking period CKH/STH stop OFF (Normal) | ○ | ○ |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | V blanking period CKH/STH stop ON | ○ | |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | H blanking period CKH stop OFF (Normal) | ○ | ○ |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | H blanking period STH stop ON | ○ | |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | X | X | 0 | 0 | 0 | 0 | 0 | 0 | Not used | | (00) |
| 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | HD/VD output ON | | ○ |
| 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | HD/VD output OFF (HD generation counter stop) | | |
| 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | BLHD output ON | | ○ |
| 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | BLHD output OFF(BLHD generation counter stop) | | |
| 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Backlight OFF (BLSW = 3V) | | ○ |
| 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | Backlight ON (BLSW = 0V) | | |
| 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | X | 0 | 0 | 0 | Not used | | (0) |
| 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Normal mode | | ○ |
| 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | For test. Do not set. | | |
| 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | X | 0 | 0 | 0 | 0 | 0 | Not used | | (0) |
| 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Normal mode | | ○ |
| 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | For test. Do not set. | | |
| 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Horizontal system counter operation | | ○ |
| 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Horizontal system counter stop (effective at standby only) | | |
| 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | X | X | X | X | X | X | X | X | Not used | | (00000000) |
| 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | X | X | X | X | X | X | X | X | Not used | | (00000000) |
| 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | X | X | X | X | X | X | X | X | Not used | | (00000000) |
| 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | X | X | X | X | X | X | X | X | Not used | | (00000000) |
| 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | X | X | X | X | X | X | X | X | Not used | | (00000000) |

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(4-1) Various mode settings 3

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Description | V latch | Default |
|-----|-----|-----|-----|-----|-----|----|----|----|----|----|----|----|----|----|----|---|---------|---------|
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Not used | | |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | Sleep mode (Note 6) | Note 6 | ○ |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | Standby mode (Note 6) | Note 6 | |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | Not used | | |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | Normal mode (Note 6) | Note 6 | |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | Not used | | |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | Not used | | |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | Not used | | |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Blanking at transfer to normal ON | | ○ |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | Blanking at transfer to normal OFF | | |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Blanking period at transfer to normal changed to 0.25 sec | | ○ |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | Blanking period at transfer to normal changed to 0.5 sec | | |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | X | X | X | 0 | 0 | 0 | 0 | 0 | Not used | | (000) |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Sample hold phase SHS1 (Note 5) | | |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | Sample hold phase SHS2 (Note 5) | | |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | Sample hold phase SHS3 (Note 5) | | |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | Sample hold phase SHS4 (Note 5) | | ○ |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | Sample hold phase SHS5 (Note 5) | | |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | Sample hold phase SHS6 (Note 5) | | |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | × | Sample hold phase, ALL through (Note 5) | | |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Normal mode | | ○ |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | For test. Do not set. | | |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | X | 0 | 0 | 0 | 0 | Not used | | |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | X | 0 | 0 | 0 | 0 | 0 | Not used | | |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Normal mode | | ○ |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | For test. Do not set. | | |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | For test. Do not set. | | |

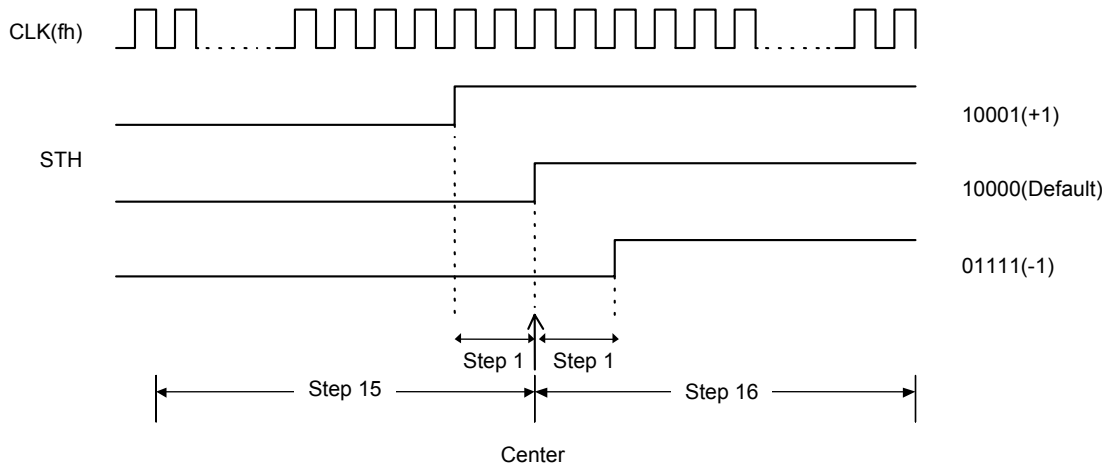
(4-2) Electronic volume setting

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Description | Default | |
|-----|-----|-----|-----|-----|-----|----|----|-----|-----|-----|-----|-----|-----|-----|-----|-------------|--------------------------|----------|
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | DA7 | DA6 | DA5 | DA4 | DA3 | DA2 | DA1 | DA0 | Not used | | |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | DA7 | DA6 | DA5 | DA4 | DA3 | DA2 | DA1 | DA0 | Not used | | |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | DA7 | DA6 | DA5 | DA4 | DA3 | DA2 | DA1 | DA0 | BRIGHT adjustment | 10010101 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | DA7 | DA6 | DA5 | DA4 | DA3 | DA2 | DA1 | DA0 | CONTRAST adjustment | 10001100 |
| 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | DA7 | DA6 | DA5 | DA4 | DA3 | DA2 | DA1 | DA0 | R-BRIGHT adjustment | 10000000 |
| 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | DA7 | DA6 | DA5 | DA4 | DA3 | DA2 | DA1 | DA0 | B-BRIGHT adjustment | 10000000 |
| 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | DA7 | DA6 | DA5 | DA4 | DA3 | DA2 | DA1 | DA0 | γ-1 adjustment | 01100100 |
| 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | DA7 | DA6 | DA5 | DA4 | DA3 | DA2 | DA1 | DA0 | γ-2 adjustment | 00000000 |
| 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | DA7 | DA6 | DA5 | DA4 | DA3 | DA2 | DA1 | DA0 | Not used | |
| 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | DA7 | DA6 | DA5 | DA4 | DA3 | DA2 | DA1 | DA0 | R-CONT adjustment | 10000000 |
| 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | DA7 | DA6 | DA5 | DA4 | DA3 | DA2 | DA1 | DA0 | B-CONT adjustment | 10000000 |
| 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | DA7 | DA6 | DA5 | DA4 | DA3 | DA2 | DA1 | DA0 | BLKLIMIT adjustment | 10000000 |
| 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | DA7 | DA6 | DA5 | DA4 | DA3 | DA2 | DA1 | DA0 | Not used | |
| 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | DA7 | DA6 | DA5 | DA4 | DA3 | DA2 | DA1 | DA0 | Not used | |
| 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | DA7 | DA6 | DA5 | DA4 | DA3 | DA2 | DA1 | DA0 | Not used | |
| 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | DA7 | DA6 | DA5 | DA4 | DA3 | DA2 | DA1 | DA0 | VCO adjustment | 10000000 |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | × | × | × | × | DA3 | DA2 | DA1 | DA0 | WHTLIMIT adjustment | 0000 |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | DA7 | DA6 | DA5 | DA4 | DA3 | DA2 | DA1 | DA0 | COM amplitude adjustment | 10000000 |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | × | × | DA5 | DA4 | DA3 | DA2 | DA1 | DA0 | COM level adjustment | 100000 |
| 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | DA7 | DA6 | DA5 | DA4 | DA3 | DA2 | DA1 | DA0 | For test. Do not set. | |

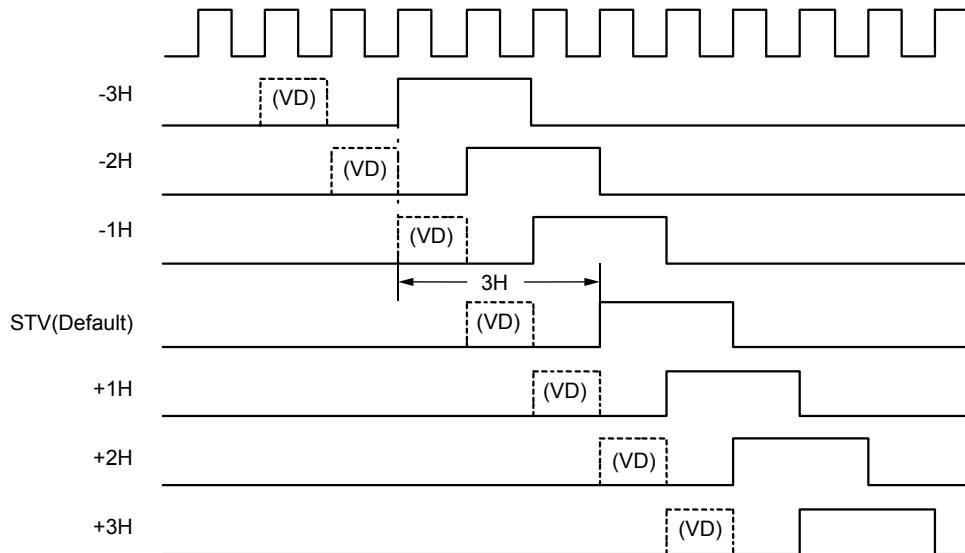
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(Note 1) H-Position set

(1Step = $2 \times 1/f_h$) : $1/f_h \approx 90\text{ns}$ <at 110,000/130,000 mode>
 : $1/f_h \approx 160\text{ns}$ <at 70,000 mode>

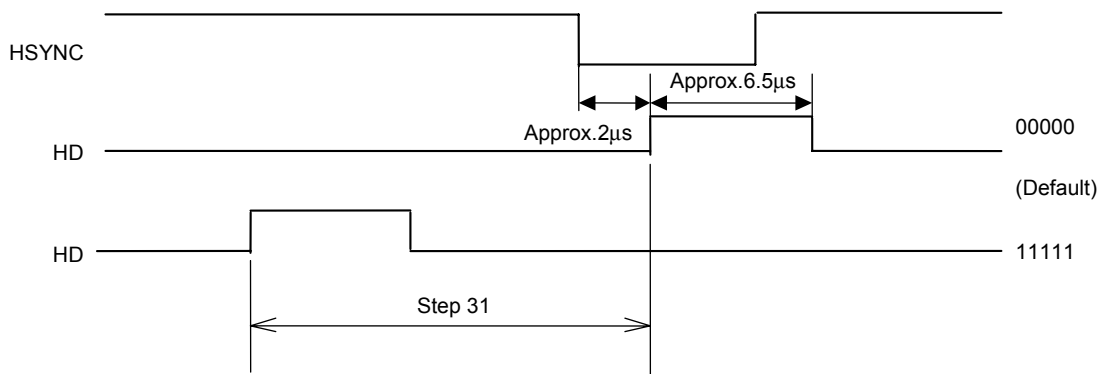


(Note 2) V-Position set



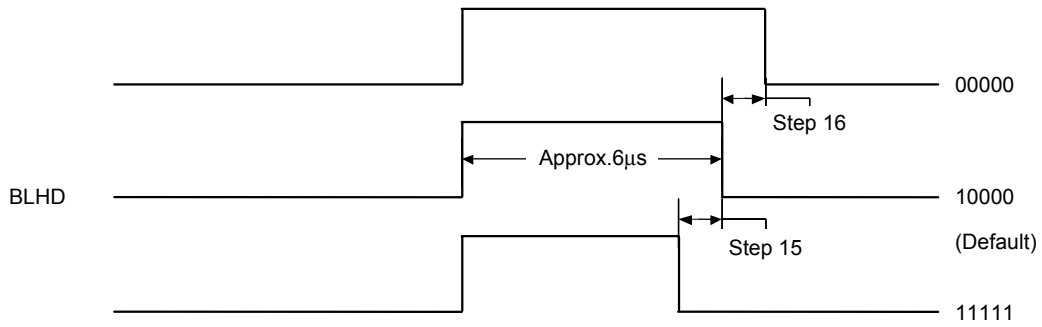
(Note 3) HD phase set

(1Step = $4 \times 1/f_h$)

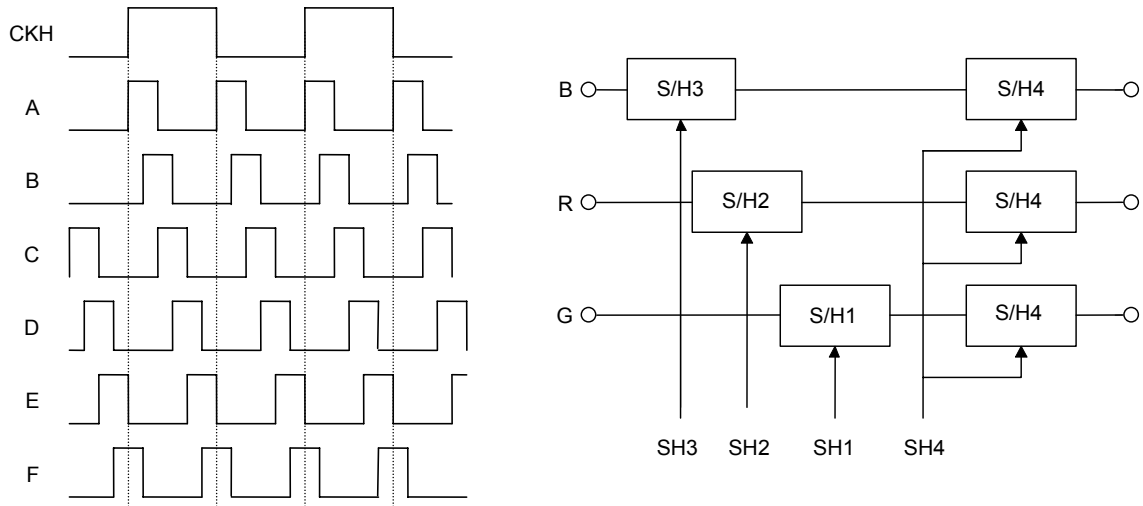


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(Note 4) BLHD phase set
 (1Step = 2×1/fh)



(Note 5) Sample hold phase
 S/H pulse timing



CSH = H (Normal)

| | SHS1 | SHS2 | SHS3 | SHS4 | SHS5 | SHS6 |
|-----|---------|---------|---------|---------|---------|---------|
| SH1 | C | B | A | F | E | D |
| SH2 | through | through | through | through | through | through |
| SH3 | A | F | E | D | C | B |
| SH4 | E | D | C | B | A | F |

CSH = L (Inverted)

| | SHS1 | SHS2 | SHS3 | SHS4 | SHS5 | SHS6 |
|-----|---------|---------|---------|---------|---------|---------|
| SH1 | C | B | A | F | E | D |
| SH2 | A | F | E | D | C | B |
| SH3 | through | through | through | through | through | through |
| SH4 | E | D | C | B | A | F |

SH1 : SH pulse for G signal SH2 : SH pulse for R signal
 SH3 : SH pulse for B signal SH4 : SH pulse for RGB signal

(Note 6) Power save function

a) Signal output in each mode

| Output Pin | Normal | Standb | Sleep |
|------------|---------------|---------------|---------|
| RGBout | Normal output | all OFF | |
| DSD | | | |
| COM | | | |
| CKH1 | Normal output | CKH1 = H | all "L" |
| CKH2 | | CKH2 = L | |
| STH | | STH = H | |
| XSTH | | XSTH = L | |
| DSG | | DSG = H | |
| XDSG | | XDSG = L | |
| ENB | | ENB = H | |
| XENB | | XENB = L | |
| CKV1 | | CKV1 = H * | |
| CKV2 | | CKV2 = L * | |
| STV | | STV = H * | |
| XSTV | | XSTV = L * | |
| HD | | Normal output | |
| VD | | | |
| BLHD | | | |
| BLSW | Normal output | | |

* After transfer from normal to standby, the respective state becomes effective after normal output for the 1V period.

b) Transfer/return to each mode

- Transfer/return between normal and standby modes is acknowledged with the vertical synchronous signal.
- Transfer/return between standby and sleep modes is changed over each time the serial data is transmitted.

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